

January 1996

LM1203A
150 MHz RGB Video Amplifier System

General Description

The LM1203A is an improved version of the popular LM1203 wideband video amplifier system. The device is intended for high resolution RGB CRT monitors. In addition to three matched video amplifiers, the LM1203A contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain or providing gain trim capability for white balance. The LM1203A also contains a voltage reference for the video inputs. The LM1203A is pin and function compatible with the LM1203.

Features

- Three wideband video amplifiers 150 MHz @ −3 dB
- Matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for individual gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver

Improvements over LM1203

- 150 MHz vs 70 MHz bandwidth
- V_{OUT} low: 0.15V vs 0.9V
- t_r, t_f: 4 ns vs 7 ns
- Built in power down spot killer

Applications

- High resolution RGB CRT monitors
- Video AGC amplifiers
- Wideband amplifiers with gain and DC offset controls

Block and Connection Diagrams

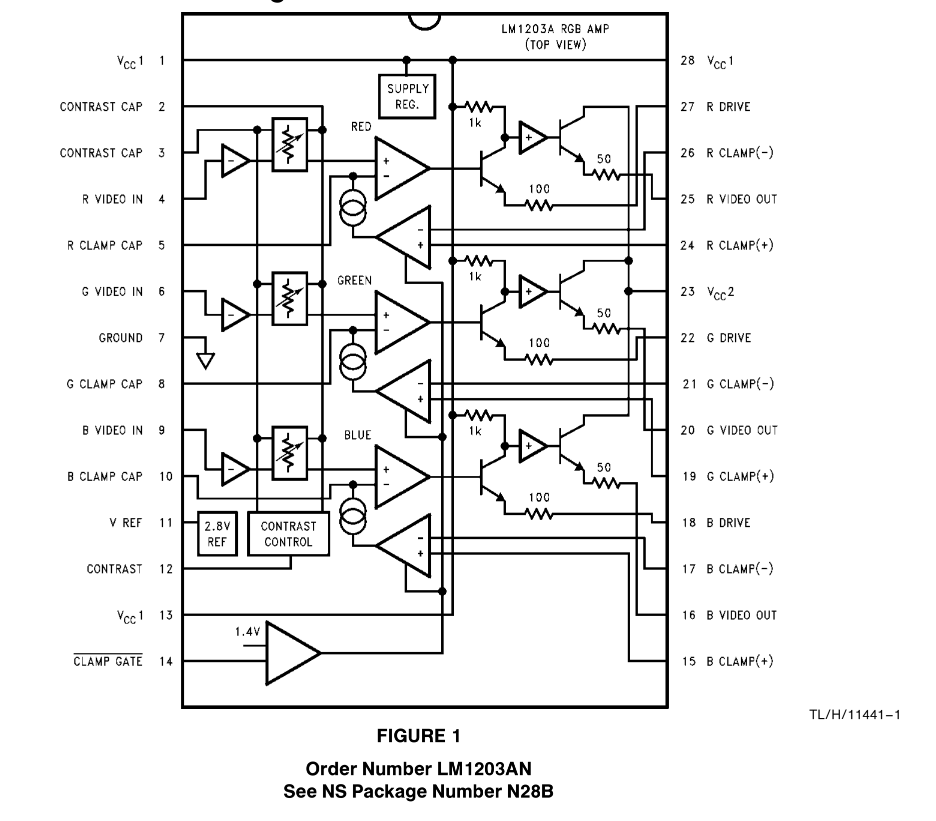


FIGURE 1

Order Number LM1203AN
See NS Package Number N28B

 RRD-B30M66/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) Pins 1, 13, 23, 28 (Note 3)	13.5V
Peak Video Output Source Current (Any One Amp) Pins 16, 20 or 25	28 mA
Voltage at Any Input Pin (V_{IN})	$V_{CC} \geq V_{IN} \geq$ GND
Power Dissipation, (P_D) (Above 25°C derate based on θ_{JA} and T_J)	2.5W
Thermal Resistance (θ_{JA})	50°C/W
Junction Temperature (T_J)	150°C
ESD Susceptibility (Note 4)	2 kV
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	265°C

Operating Ratings (Note 2)

Temperature Range	−20°C to +80°C
Supply Voltage (V_{CC})	$10.8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics

See Test Circuit *(Figure 2)*, T_A = 25°C; $V_{CC1} = V_{CC2}$ = 12V. S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	$V_{CC1} + V_{CC2}$, $R_L = \infty$ (Note 7)	70	95	mA (max)
V11	Video Input Reference Voltage		2.8	2.5	V (min)
				3.1	V (max)
I_B	Video Input Bias Current	Any One Amplifier	7	20	μA (max)
V_{14L}	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8	V (max)
V_{14H}	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0	V (min)
I_{14L}	Clamp Gate Low Input Current	V14 = 0V	−1	−5.0	μA (max)
I_{14H}	Clamp Gate High Input Current	V14 = 12V	0.07	0.2	μA (max)
I_{CLAMP+}	Clamp Cap Charge Current	V5, 8 or 10 = 0V	750	500	μA (min)
I_{CLAMP-}	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	−750	−500	μA (min)
V_{OL}	Video Output Low Voltage	V5, 8 or 10 = 0V	0.15	0.5	V (max)
V_{OH}	Video Output High Voltage	V5, 8 or 10 = 5V	7.5	7	V (min)
$\Delta V_{O(2V)}$	Video Output Offset Voltage	Between Any Two Amplifiers, V15 = 2V	2	±25	mV (max)
$\Delta V_{O(4V)}$	Video Output Offset Voltage	Between Any Two Amplifiers, V15 = 4V	2	±25	mV (max)

AC Electrical Characteristics

See Test Circuit *(Figure 2)*, T_A = 25°C; V_{CC1} = V_{CC2} = 12V. S17, 21, 26 Closed; V14 = 0V; V15 = 4V unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$A_{V\ max}$	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mV_{PP}	6.5	4.5	V/V (min)
$\Delta A_{V\ 5V}$	Attenuation @ 5V	Ref: A_V max, V12 = 5V	−8		dB
$\Delta A_{V\ 2V}$	Attenuation @ 2V	Ref: A_V max, V12 = 2V	−30		dB
$A_{V\ match}$	Absolute Gain Match @ A_V max	V12 = 12V (Note 8)	±0.3		dB
$\Delta A_{V\ track\ 1}$	Gain Change Between Amplifiers	V12 = 5V (Notes 8, 9)	±0.1		dB
$\Delta A_{V\ track\ 2}$	Gain Change Between Amplifiers	V12 = 5V (Notes 8, 9)	±0.3		dB
THD	Video Amplifier Distortion	V12 = 3V, V_O = 1 V_{PP}	1		%
f (−3 dB)	Video Amplifier Bandwidth (Notes 10, 11)	V12 = 12V, V_O = 4 V_{PP} (No External Peaking Capacitor)	100		MHz
f (−3 dB)	Video Amplifier Bandwidth (Notes 10, 11)	V12 = 12V, V_O = 4 V_{PP} With 18 pF Peaking Cap from Pins 18, 22 and 27 to GND	150		MHz
t_r	Output Rise Time (Note 10)	V_O = 4 V_{PP} (No External Peaking Capacitor)	3		ns
t_f	Output Fall Time (Note 10)	V_O = 4 V_{PP} (No External Peaking Capacitor)	4		ns
$V_{sep\ 10\ kHz}$	Video Amplifier 10 kHz Isolation	V12 = 12V (Note 12)	−70		dB
$V_{sep\ 10\ MHz}$	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 10, 12)	−50		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: The supply current specified is the quiescent current for V_{CC1} and V_{CC2} with R_L = ∞, see *Figure 2's* test circuit. The supply current for V_{CC2} (pin 23) also depends on the output load. With video output at 2V DC, the additional current through V_{CC2} is 18 mA for *Figure 2's* test circuit.

Note 8: Measure gain difference between any two amplifiers. V_{IN} = 1 V_{PP}.

Note 9: Δ $A_{V\ track}$ is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage (V12) at either 5V or 2V measured relative to an A_V max condition, V12 = 12V. For example, at A_V max the three amplifiers' gains might be 17.4 dB, 16.9 dB and 16.4 dB and change to 7.3 dB, 6.9 dB, and 6.5 dB respectively for V12 = 5V. This yields the measured typical ±0.1 dB channel tracking.

Note 10: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video amplifier 10 MHz isolation test also requires this printed circuit board.

Note 11: Adjust input frequency from 10 kHz (A_V max reference level) to the −3 dB corner frequency ($f_{-3\ dB}$).

Note 12: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for V_{sep} = 10 MHz.

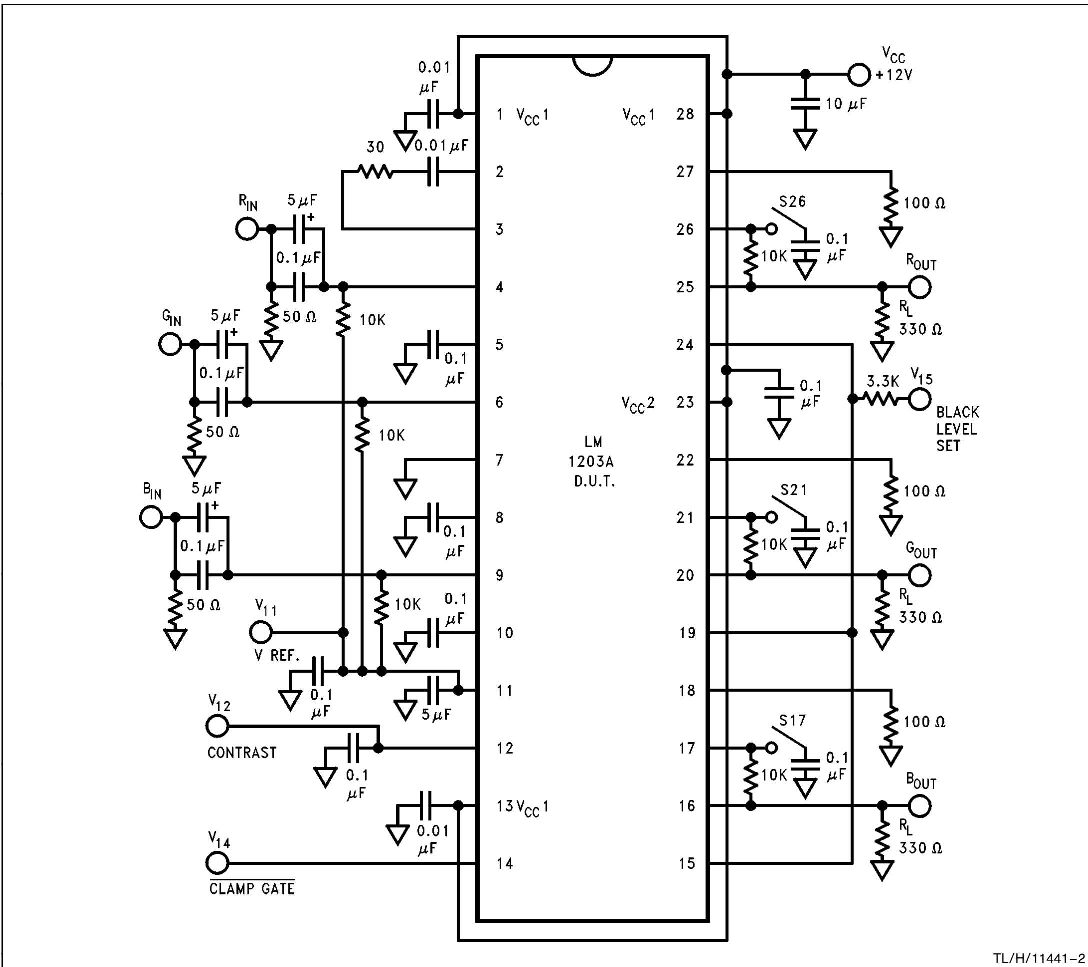
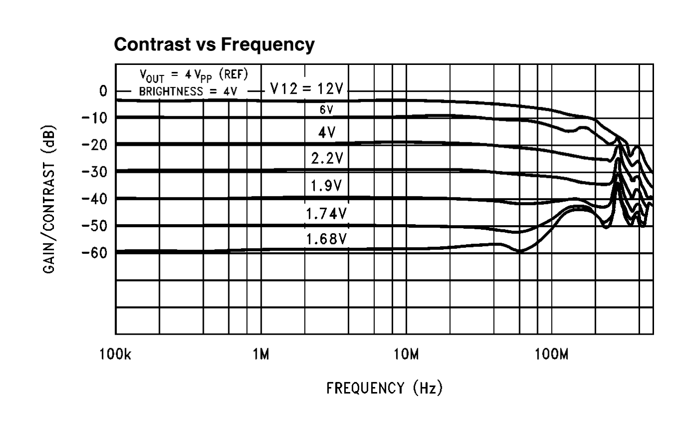


FIGURE 2. LM1203A Test Circuit

Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified

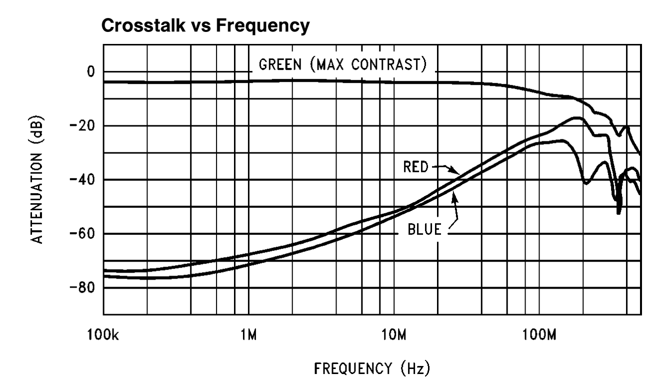
Contrast vs Frequency





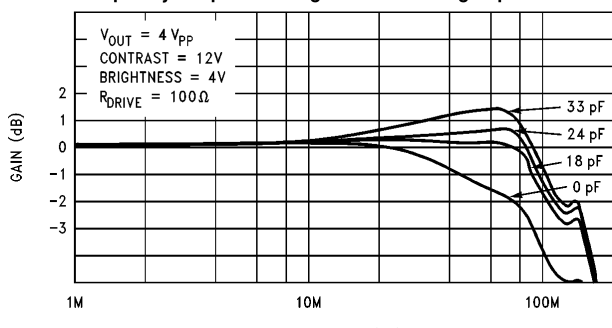
Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified (Continued)

Crosstalk vs Frequency



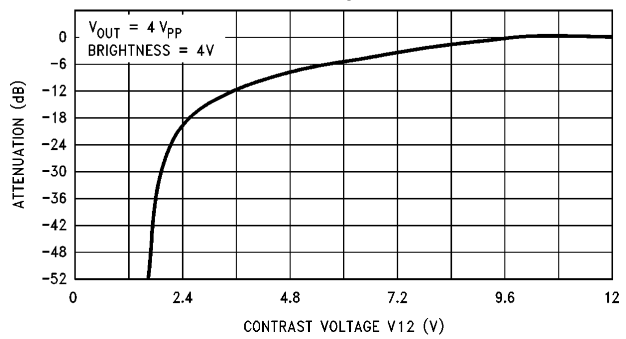
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Frequency Response Using Various Peaking Caps

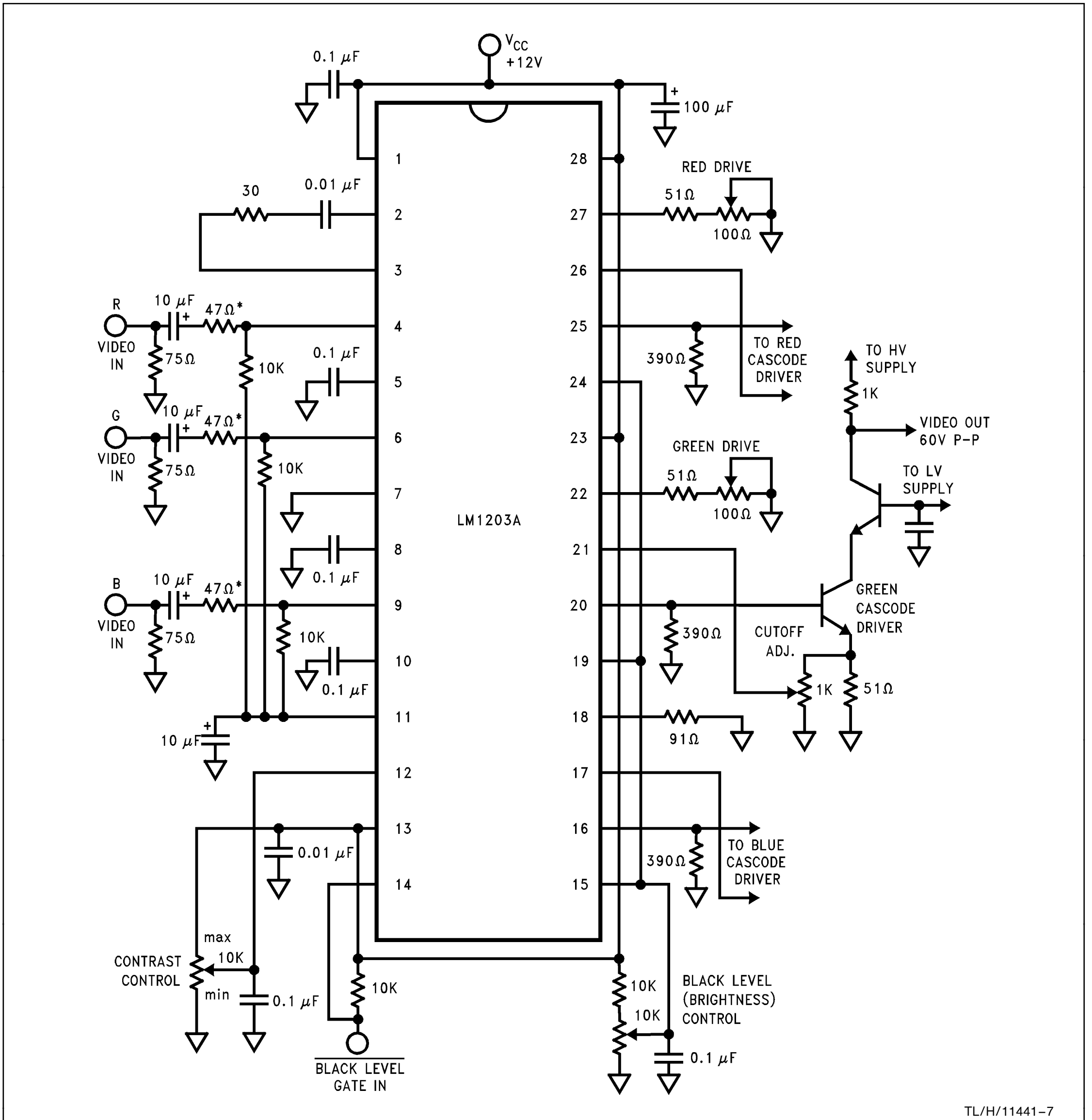


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Attenuation vs Contrast Voltage



TL/H/11441–6



*47Ω resistors are added to the input pins for protection against current surges coming from the 10 µF capacitors. By increasing these resistors to well over 100Ω the rise and fall times of the LM1203A can be increased for EMI considerations.

FIGURE 3. LM1203A Typical Application

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally AC coupled to the video amplifiers. These input signals are approximately 1V peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203A which contains the three matched video amplifiers, contrast control and brightness control.

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a DC-operated attenuator which varies the AC gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the DC bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

VIDEO AMPLIFIER SECTION

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled and all external components are shown outside the dashed line. The video input is applied to pin 6 via a 10 μF coupling capacitor. DC bias for the video input is through the 10k resistor connected to the 2.8V reference at pin 11. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. Q2's collector current is then directed to the V_{CC1} supply directly or through the 2k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. This differential DC voltage is generated by the contrast control circuit which is described in the following sections. A 0.01 μF decoupling capacitor in series with a 30Ω resistor is required between pins 2 and 3 to ensure high frequency isolation between the three video amplifiers which share these common connections. The video signal is buffered by Q5 and Q6 and DC level shifted by the voltage drop across R5. The magnitude of the current through R5 is determined by the voltage at pin 8. The voltage at pin 8 is set by the clamp comparator output current which charges or discharges the clamp hold capacitor during the black level period of the video waveform. Transistors Q9 and Q10 are Darlington connected to ensure a minimum discharge of the clamp hold capacitor during the time that the clamp capacitor is gated off. Q7, Q8 and R6 form a current mirror which sets a voltage at the base of Q11. Q11 buffers the video signal to the base of Q12 which provides additional signal gain. The "Drive" pin allows the user to trim the Q12 gain of each amplifier to correct for gain differences in the CRT and high voltage cathode driver gain stages. A small capacitor (several pico-Farads) from the "Drive" pin to ground will cause high frequency peaking and slightly improve the amplifier's bandwidth.

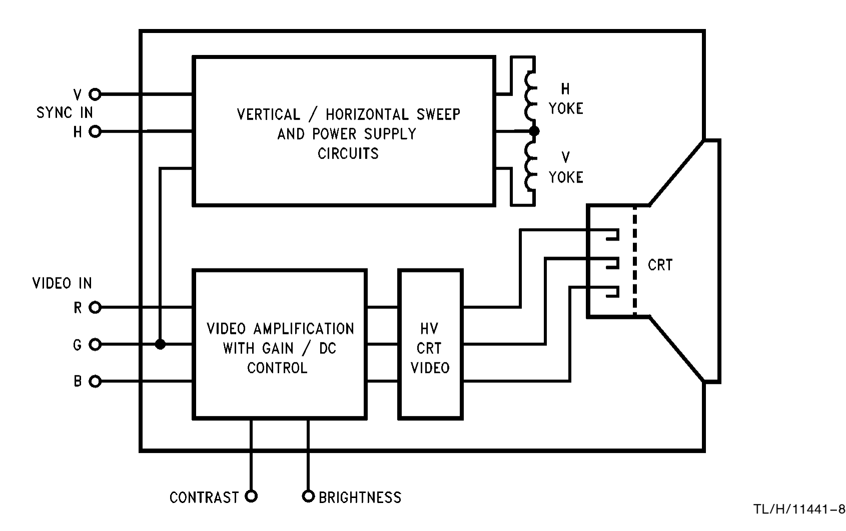


FIGURE 4. Typical RGB Color Monitor Block Diagram

Circuit Description (Continued)

For individual gain adjustment of each video channel, a 51Ω resistor in series with a 100Ω potentiometer should be used with the red and green channel drive pins. A 91Ω resistor used with the blue channel drive pin sets the blue channel amplifier gain at approximately 6.2. The 100Ω potentiometer at the red and green channel drive pins allow a gain of 6.2 with ±25% gain adjustment. The video signal at the collector of Q12 is buffered and level shifted down by Q13, Q14 and Q15 to the base of the output emitter follower Q16. A 50Ω decoupling resistor is included in series with the emitter of Q16 and the video output pin so as to prevent oscillations when driving capacitive loads. An external resistor should be connected between the video output pin and ground. The value of this resistor should not be less than 390Ω or else package power limitations may be exceeded under worst case conditions (high supply voltage, maximum current, maximum temperature). The collector current from the video output transistor of each video channel is returned to the power supply at V_{CC2}, pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC1} and V_{CC2} supply current at 12V supply voltage with no pull down resistor at the output (i.e., $R_L = \infty$, see test circuit *Figure 2*). The IC power dissipation due to V_{CC2} is dependant upon the external video output pull down resistor.

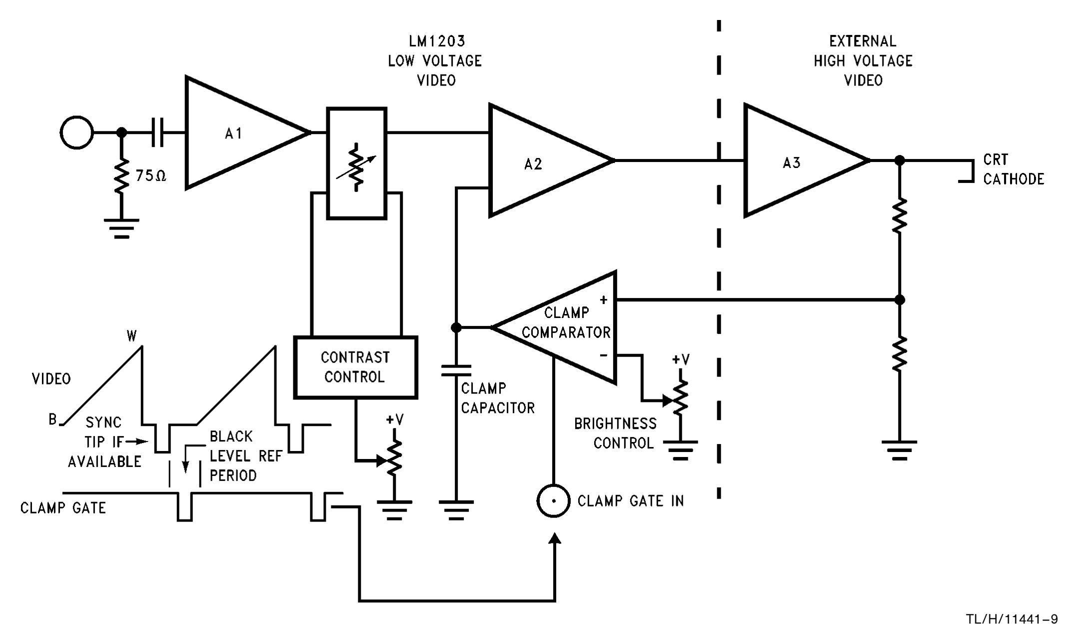


FIGURE 5. Block Diagram of LM1203A Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)

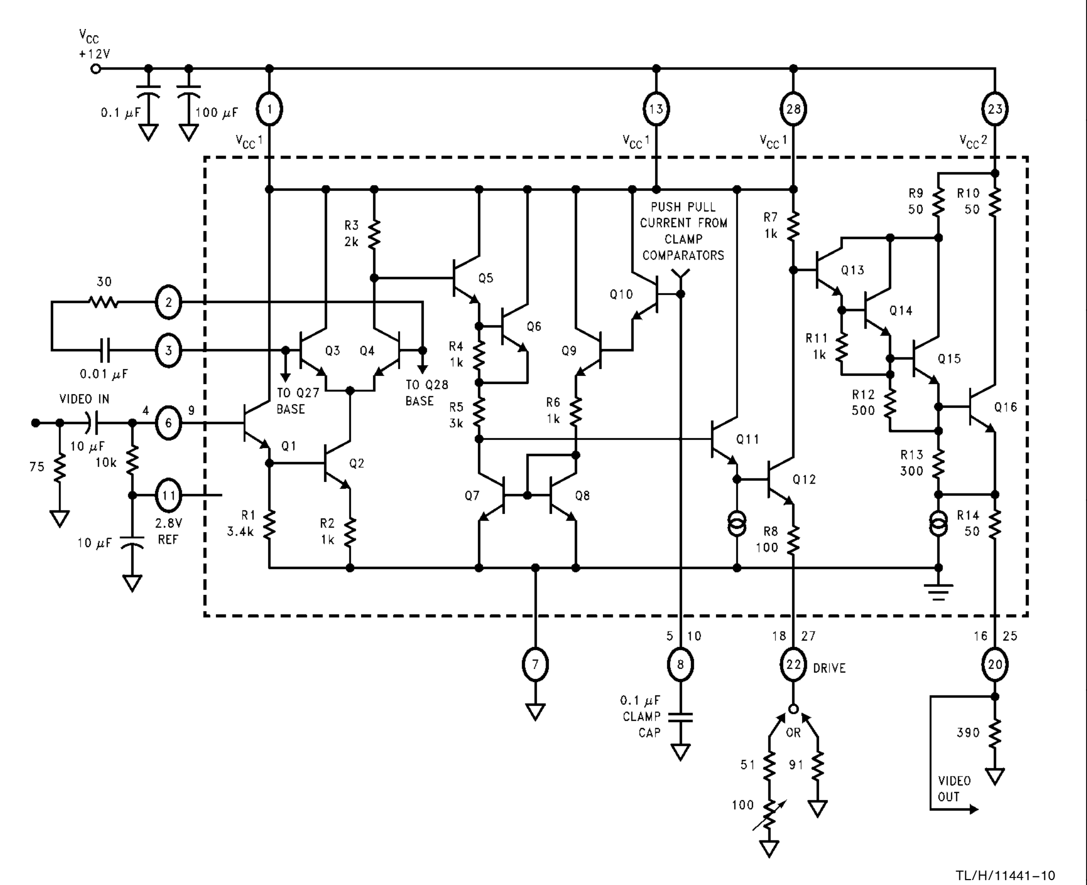


FIGURE 6. Simplified Schematic of LM1203A Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

INPUT REFERENCE AND CONTRAST CONTROL SECTION

Figure 7 shows the input reference and contrast control circuitry. A temperature compensated 2.8V reference voltage is made available at pin 11. The external DC biasing resistors shown should not be larger than 10k because minor differences in input bias currents of the individual video amplifiers may cause offsets in gain. *Figure 7* also shows how the contrast control circuit is configured. R21, R22, Q22, Q23 and Q24 establish a low impedance zero TC half supply voltage reference at the base of Q25. The differential amplifier formed by Q27, Q28 and feedback transistor Q29 along with R28 and R29 establish a differential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q28, a new differential voltage is generated that reflects the change in the ratio of currents in Q27 and Q28. To allow voltage control of the current through Q28, resistor R27 is added between the collector Q28 and pin 12. A capacitor should be connected from pin 12 to ground to prevent noise from the contrast control potentiometer from entering the IC.

CLAMP GATE AND CLAMP COMPARATOR SECTION

Figures 8 and *9* show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit *(Figure 8)* consists of a PNP input buffer transistor (Q46), a PNP emitter coupled pair (Q47 and Q49) referenced on one side to 2.1V and an output switch transistor Q53. When the clamp gate input at pin 14 is high (>1.5V) the Q53 switch is on and shunts the 200 µA current from current source Q54 to ground. When pin 14 is low (<1.3V) the Q53 switch is off and the 200 µA current is mirrored by the current mirror comprised of Q55 and Q36 (see *Figure 9*). Consequently the clamp comparator comprised of the differential pair Q35 and Q37 is enabled. The input of each clamp comparator is similar to the clamp gate except than an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitors at pins 5, 8 and 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, a resistor (R37) with a value one half that of R36 or R39 is connected between the bases of Q34 and Q38. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

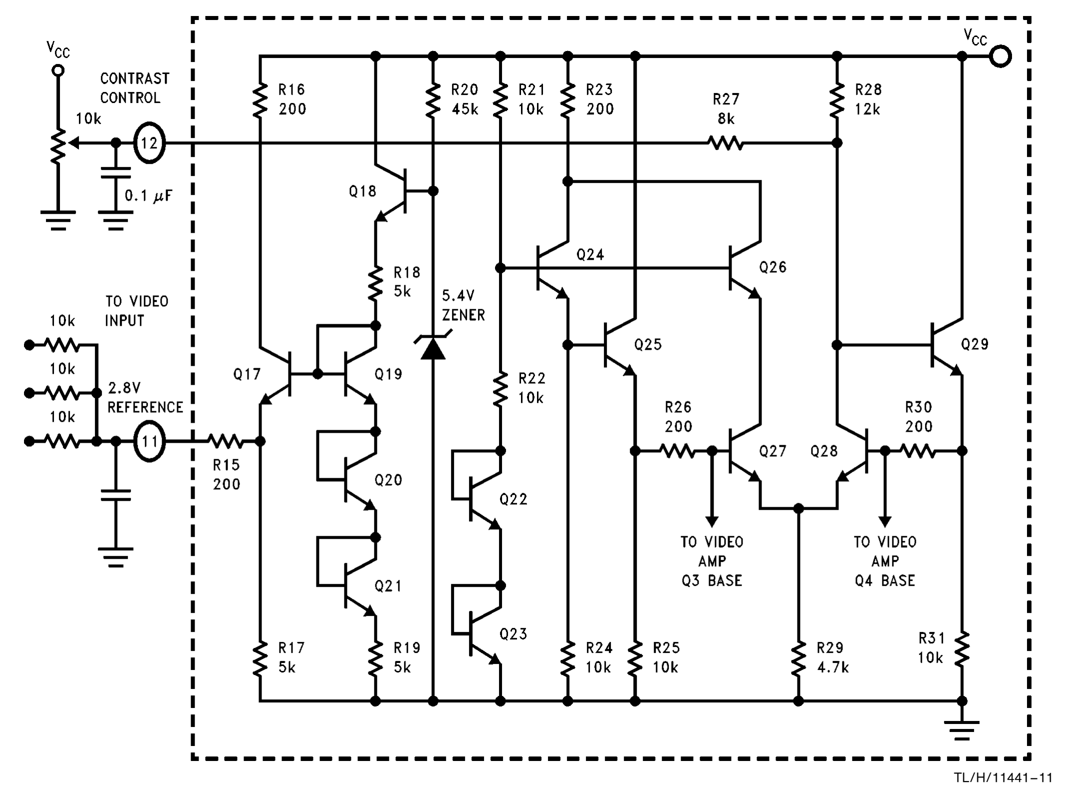


FIGURE 7. Simplified Schematic of LM1203A Video Input Reference and Contrast Control Circuits

Circuit Description (Continued)

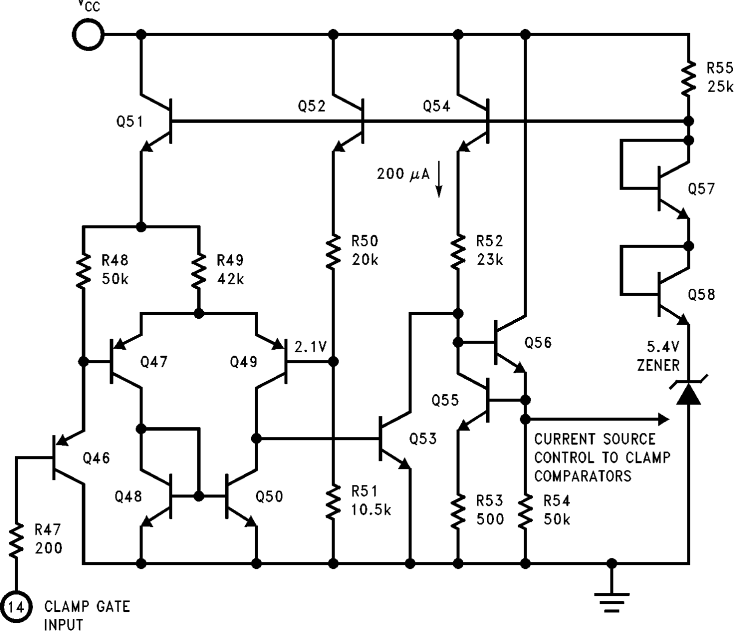


FIGURE 8. Simplified Schematic of LM1203A Clamp Gate Circuit

Circuit Description (Continued)

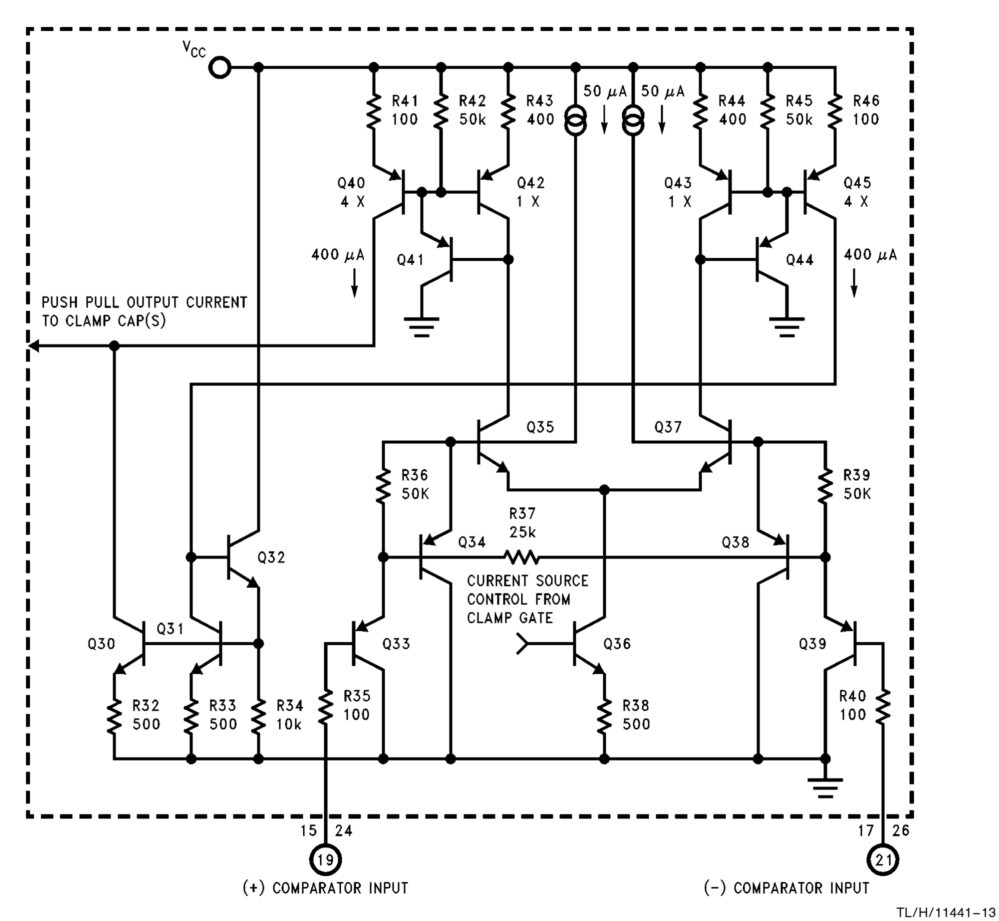


FIGURE 9. Simplified Schematic of LM1203A Clamp Comparator Circuits

Additional Applications of the LM1203A

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0Ω and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

Figure 11 shows a complete RGB video preamplifier circuit using the LM1203A. A quad Exclusive-OR gate (MM74HC86) is used to generate the back porch clamp signal from the composite sync input signal. The composite H Sync input signal may have either polarity. The back porch clamp signal applied to LM1203A's pin 14 allows clamping the video output signals to the black reference level, thereby providing DC restoration. The back porch clamp pulse width is determined by the time constant due to the product of R11 and C15. For fast horizontal scan rates, the back porch clamp pulse width can be made narrower by decreasing the value of R11 or C15 or both. Note that an MM74C86 Exclusive-OR gate may also be used, however, the pin out is different than that of the MM74HC86.

For optimum performance and maximum bandwidth, high speed buffer transistors (Q1, Q2 and Q3 in *Figure 11*) are recommended. The 2N5770 NPN transistors maintain high speed at high currents when driving the inputs of high voltage CRT drivers.

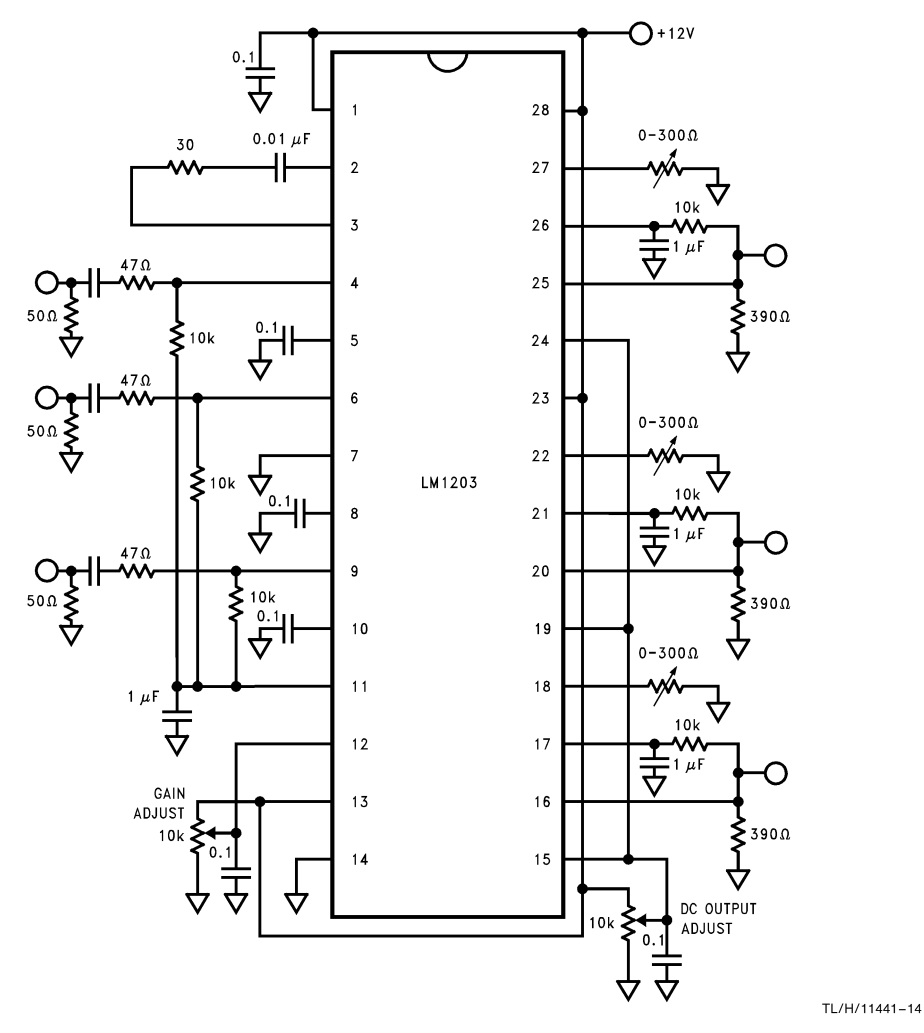


FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Application)

Additional Applications of the LM1203A (Continued)

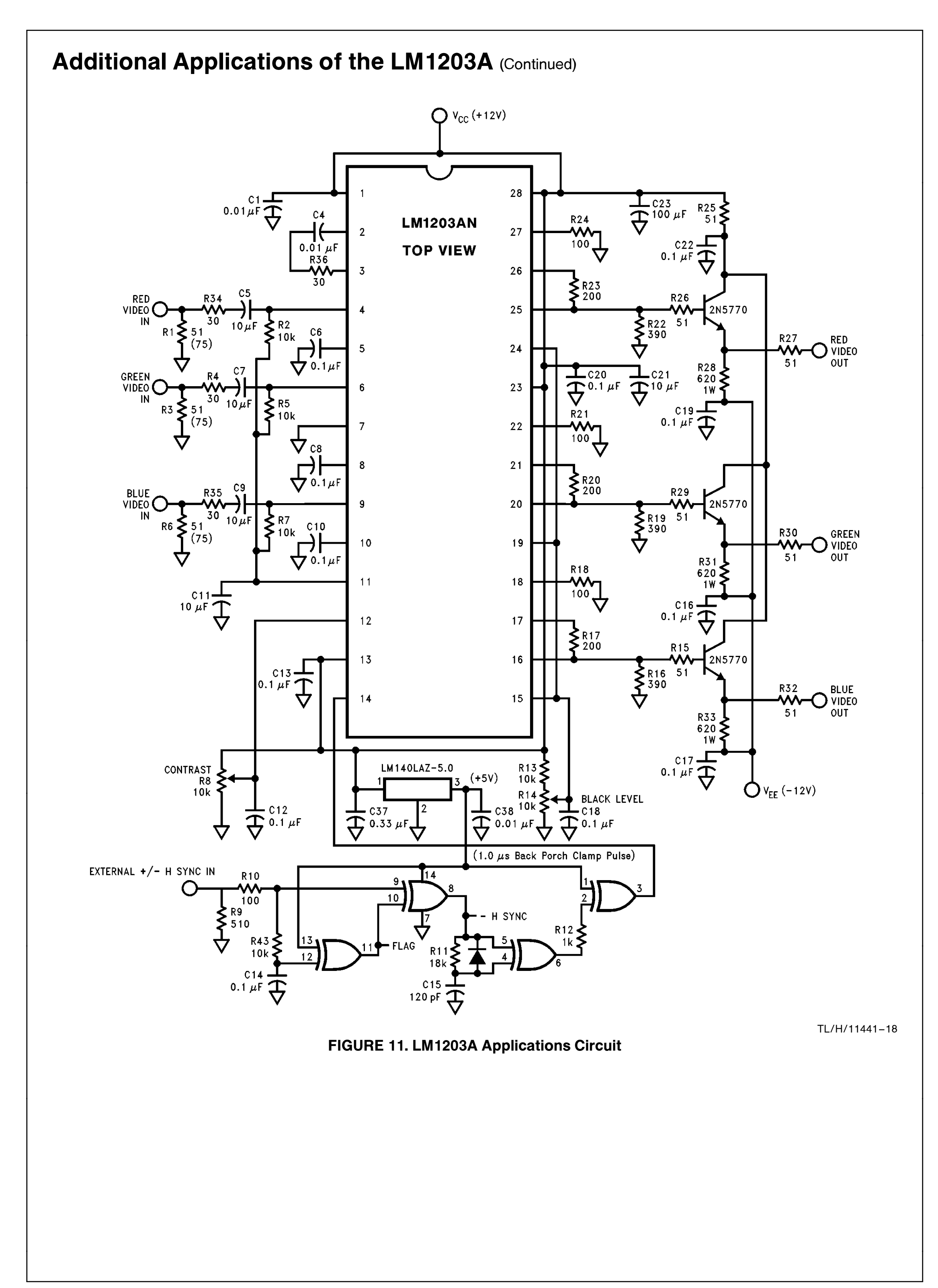


FIGURE 11. LM1203A Applications Circuit

LM1203A vs LM1203

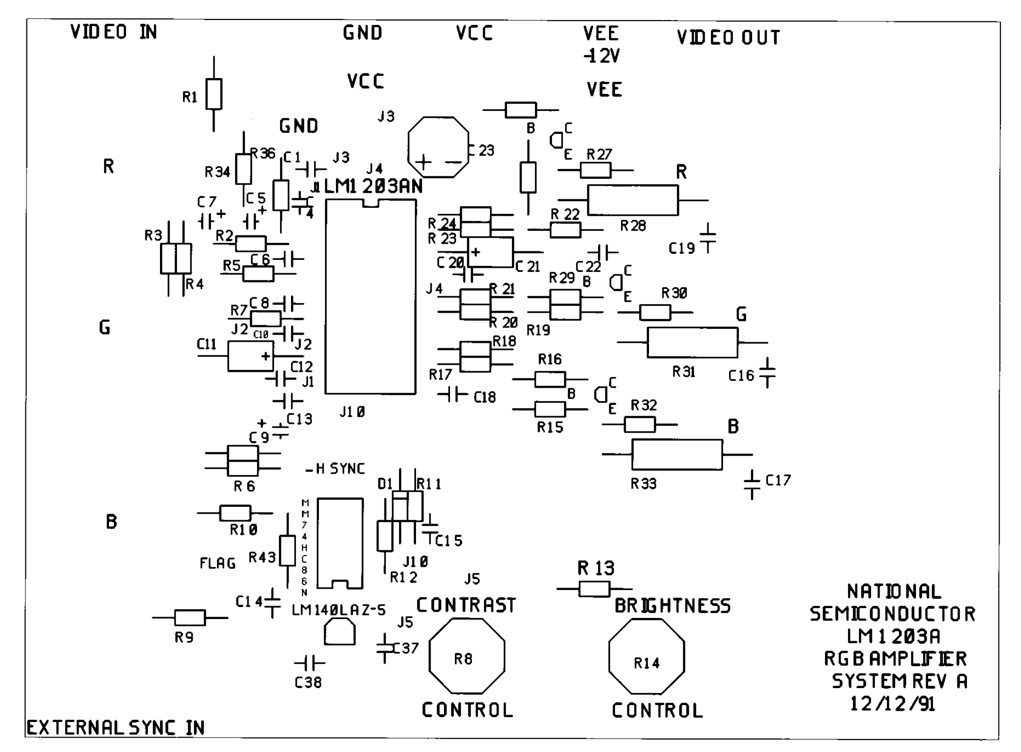
LM1203A is an improved version of the LM1203 RGB video amplifier system and is pin and function compatible with the LM1203. LM1203A's output voltage can swing as low as 0.15V as opposed to 0.9V for the LM1203. This eliminates the need for a level shift stage between the preamplifier and the CRT driver in most applications.

The LM1203A also offers faster rise and fall times of 4 ns vs 7 ns for the LM1203 and 100 MHz bandwidth vs 70 MHz for LM1203. With a peaking capacitor across the drive resistor, LM1203A's bandwidth can be extended to 150 MHz. Because of LM1203A's wide bandwidth, the device may oscillate if plugged directly into an existing LM1203 board. For optimum performance and stable operation, a double sided printed circuit board with adequate ground plane and power supply decoupling as close to the V_{CC} pins as possible is recommended. *Figure 12* shows the layout of the PC board for *Figure 11's* circuit. For suggestions on optimum PC board layout, please see the reference section below.

The LM1203A also includes a built-in power down spot killer to prevent a flash on the screen upon power down. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter than white level at the output of the CRT driver, thus causing a flash on the screen.

REFERENCE

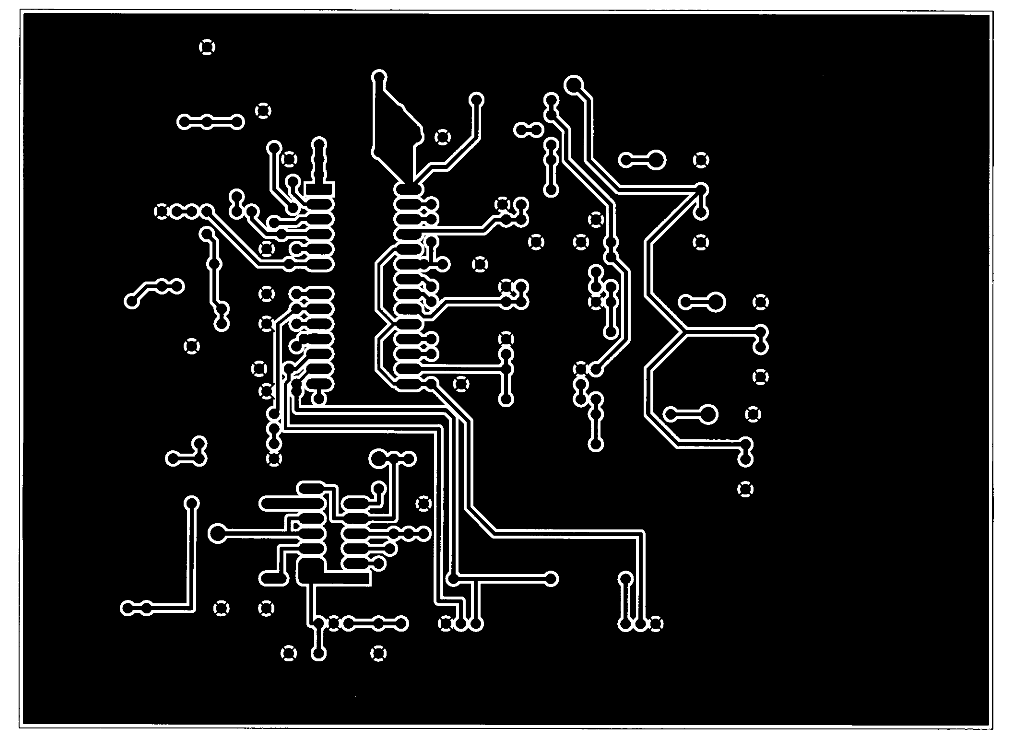
Ott, Henry W. *Noise Reduction Techniques in Electronic Systems,* John Wiley & Sons, New York, 1976.



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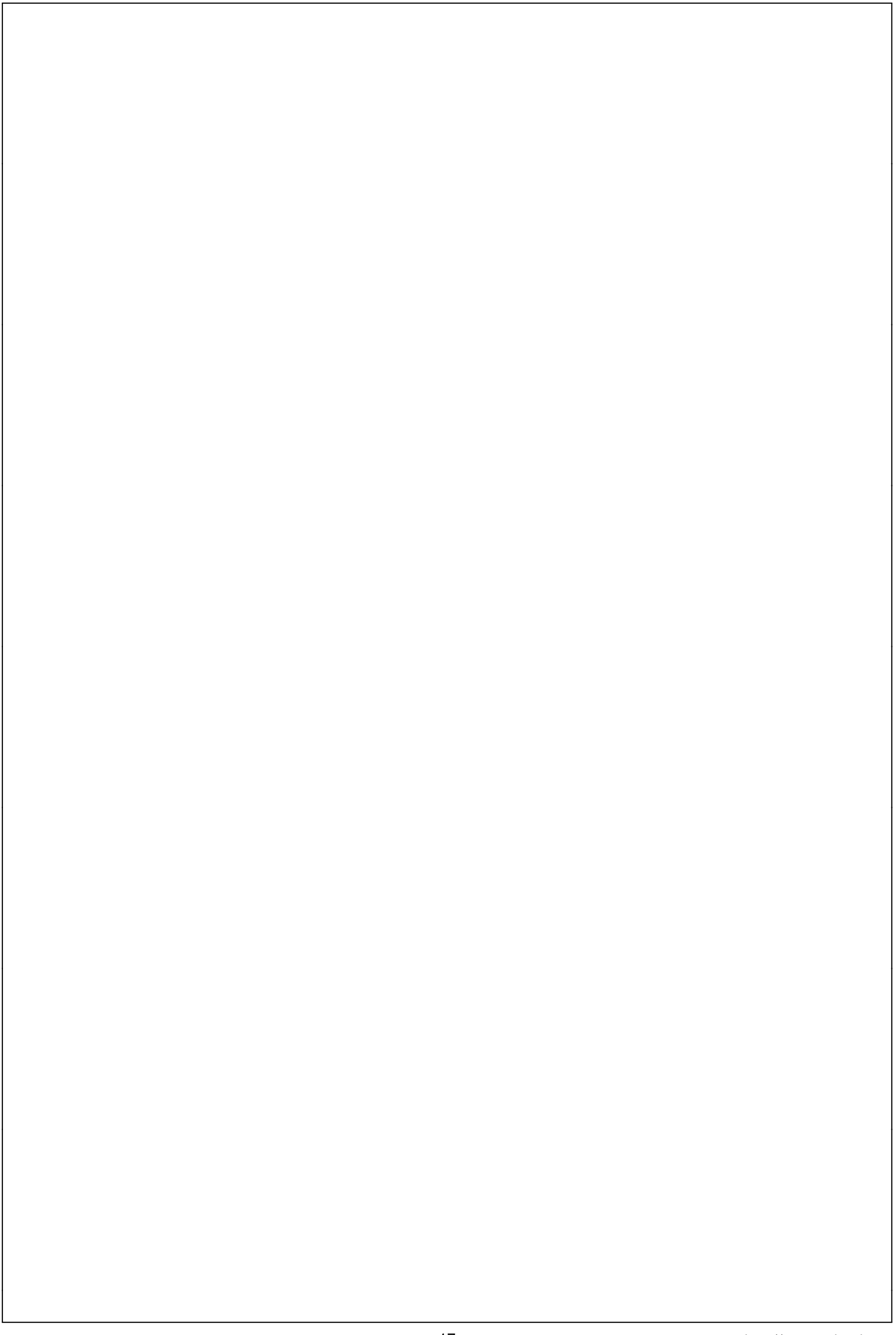
FIGURE 12(a). PC Board Silk Screen

Additional Applications of the LM1203A (Continued)



TL/H/11441–17

FIGURE 12(b). PC board layout of bottom side. Top side of PC board (not shown) is full ground plane.



Physical Dimensions inches (millimeters) unless otherwise noted

28 27 26 25 24 23 22 21 20 19 18 17 16 15

0.062 (1.575) RAD

0.510 ± 0.005 (12.95 ± 0.127)

1 2 3 4 5 6 7 8 9 10 11 12 13 14

PIN NO. 1 IDENT

1.393 − 1.420 (35.38 − 36.07)

0.030 (0.762) MAX

0.600 − 0.620 (15.24 − 15.75)

95° ± 5°

0.009 − 0.015 (0.229 − 0.381)

0.580 (14.73) MIN

0.625 +0.025 −0.015 (15.88 +0.635 −0.381)

0.145 − 0.210 (3.683 − 5.334)

0.050 (1.270) TYP

0.125 − 0.165 (3.175 − 4.191)

0.020 (0.508) MIN

86° 94° TYP

0.050 ± 0.015 (1.270 ± 0.381)

0.100 ± 0.010 (2.540 ± 0.254)

0.018 ± 0.003 (0.457 ± 0.076)

0.125 − 0.145 (3.175 − 3.683)

N28B (REV E)

Order Number LM1203AN
NS Package Number N28B

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